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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/538,456	OMATHUNA, PADRAIG	
	Examiner	Art Unit	
	KALPIT PARIKH	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The instant detailed action is in response to Applicant's submission filed on 26 January 2010.

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

I. APPLICATION INFORMATION

Application No. 10/538456 has a total of 18 claims pending in the application; there are 3 independent claims and 15 dependent claims, all of which are ready for examination by the examiner.

II. REJECTIONS NOT BASED ON PRIOR ART

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plurality of integrated circuits (ICs) disposed on a substrate and communicatively coupled to one another through test circuitry that provides debugging capabilities, and transmitting, using the test circuitry, the second set of programming instructions to a second one of the plurality of ICs must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

III. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **CLAIMS 1-5 AND 7-9** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Pat No. 5757639) in view of Stancil (US Pat No. 6272584) and May (US Pat No. 7343483).

As per claim 1, Yamada discloses a method of transferring programming instructions from a first memory disposed on a substrate, to a plurality of integrated circuits (ICs), comprising:

- a first one of the plurality of ICs (see Yamada FIG 1: 1 MASTER CPU) accessing the first memory (see Yamada FIG 6: S2), retrieving a first set of programming instructions, and storing the first set of programming instructions within the first one of the plurality of ICs (see Yamada FIG 6: S3 and COL 3 LINES 32-46); and
- the first one of the plurality of ICs accessing the first memory, retrieving a second set of programming instructions, and transmitting the second set of programming instructions to a second one of the plurality of ICs (see Yamada FIG 6: S5 and COL 3 LINES 32-46).

However, Yamada does not expressly disclose the memory and the plurality of integrated circuit (ICs) are disposed on the substrate.

In the same field of endeavor Stancil discloses it is well known to place many components on a motherboard (substrate) (see Stancil COL 5 LINES 5-10).

It would have been obvious to modify Yamada to integrate the components on a motherboard.

The suggestion/motivation for doing so would have been of higher performance system (see Stancil COL 2 LINES 24-28).

Therefore it would have been obvious to modify Yamada to integrate the components on a motherboard for the benefit higher performance to arrive at the invention as specified in the claims.

However, Yamada and Stancil does not expressly disclose

- communicatively coupled to one another through test circuitry that provides debugging capabilities,
- transmitting, using the test circuitry, the second set of programming instructions to a second one of the plurality of ICs.

In the same filed of endeavor May discloses

- communicatively coupled to one another through test circuitry that provides debugging capabilities (see May FIG 2: 240),

  [The embedded controller is construed as a first integrated circuit and the PLD array is construed as the second integrated circuit.]
- transmitting, using the test circuitry, the second set of programming instructions to a second one of the plurality of ICs (see May COL 3 LINES 24-41).

It would have been obvious to modify Yamada and Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by May.

The suggestion/motivation for doing so would have been for the benefit of a test interface and the use of an industry standard protocol (see May FIG 2: 'PLD TEST INTERFACE' and COL 3 LINES 40-45).

Therefore it would have been obvious to modify Yamada and Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by May for the benefit of a test interface to arrive at the invention as specified in the claims.

As per claim 2, Yamada in view of Stancil and May disclose the method of Claim 1,

- wherein the first and second ones of the plurality of ICs each comprise a processor capable of executing, respectively, the first and second sets of programming instructions (see Yamada FIG 6: S3, S5: 'PROGRAM DATA') and

- further including the step of debugging the plurality of ICs using the test circuitry by operating the test circuitry in a test mode (see May FIG 2: PLD TEST INTERFACE) and
- wherein each of the steps of accessing retrieving, storing and transmitting is implemented when the test circuitry is in a mode other than the test mode (see May COL 13 LINES 24-41).

As per claim 3, Yamada in view of Stancil and May disclose the method of Claim 2, further comprising

- the first one of the plurality of ICs executing at least a portion of the first set of programming instructions (see Yamada COL 3 LINES 45-55);
- in a test mode, operating the test circuitry using control signals from a source external to the substrate (see May FIG 2: PLD TEST INTERFACE) and
- in am ode other than the test mode, operating the test circuitry using control signals generated on the substrate (see May COL 13 LINES 24-41).

As per claim 4, Yamada in view of Stancil and May disclose the method of Claim 3,

- wherein executing at least a portion of the first set of programming instructions occurs prior to transmitting the second set of programming instructions to a second one of the plurality of ICs (see May COL 3 LINES 42-52).

As per claim 5, Yamada in view of Stancil and May disclose the method of Claim 2,

- further comprising the first one of the plurality of ICs accessing the first memory, retrieving a first set of data, and storing the first set of data within the first one of the plurality of ICs; and the first one of the plurality of ICs accessing the first memory, retrieving a second set of data, and transmitting the second set of data to a second one of the plurality of ICs (see Yamada FIG 6: S3, S5).

As per claim 7, Yamada in view of Stancil and May disclose the method of Claim 3,

- wherein transmitting comprises serially shifting data out from the first integrated circuit and concurrently shitting data in to the second integrated circuit (see Yamada FIG 6: S5 "SERIALLY TRANSFER").

As per claim 8, Yamada in view of Stancil and May disclose the method of Claim 7,

- further comprising transmitting control information from the first integrated circuit to the second integrated circuit prior to transmitting the second set of programming instructions to a second one of the plurality of ICs (see Yamada FIG 6: S4).

As per claim 9, Yamada in view of Stancil and May disclose the method of Claim 8,

- wherein the control information directs the second one of the plurality of ICs to receive a subsequent transmission of programming instructions (see Yamada FIG 6: S5).

3. **CLAIMS 6** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Pat No. 5757639) in view of Stancil (US Pat No. 6272584) and May (US Pat No. 7343483) as applied to claim 3 above and further in view of Sun Microelectronics (NPL: Introduction to JTAG Boundary Scan).

As per claim 6, Yamada in view of Stancil and May disclose the method of Claim 3,

- wherein the substrate comprises a printed circuit board (see Stancil COL 2 LINE 25: "motherboard"), and

However, Yamada in view of Stancil and May does not expressly disclose

- the test circuitry of each of the plurality of ICs has an input for a test mode signal and a clock that is common to each of the plurality of ICs.

In the same field of endeavor Sun Microelectronics discloses

- the test circuitry of each of the plurality of ICs has an input for a test mode signal (see Sun Microelectronics PAGE 3 2nd Paragraph) and a clock that is common to each of the plurality of ICs (see Sun Microelectronics PAGE 6 FIG 3: TCK).

It would have been obvious to modify Yamada in view of Stancil and May to communicatively couple the first and second integrated circuit through test circuitry as taught by Sun Microelectronics.

The suggestion/motivation for doing so would have been for the benefit of a test interface and the use of an industry standard protocol (see Sun Microelectronics PAGE 1 Paragraph 1: "This capability enables in-circuit testing without the need bed-of-nails in-circuit testing equipment.").

Therefore it would have been obvious to modify Yamada and Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by Sun Microelectronics for the benefit of a test interface to arrive at the invention as specified in the claims.

4. **CLAIMS 10-14** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Pat No. 5757639) in view of Stancil (US Pat No. 6272584) and Sun Microelectronics (NPL: Introduction to JTAG Boundary Scan).

As per claim 10, Yamada discloses in a system including a plurality of integrated circuits (ICs), each IC having a memory for storing at least programming instructions, and a processor coupled to the memory for executing programming instructions stored in the memory; the system further including a single non-volatile memory disposed on the printed circuit board and coupled for memory access to only a first one of the plurality of ICs, a method of downloading code from the single non-volatile memory to each of the plurality of ICs, comprising:

- receiving, at a first one of the plurality of ICs, a first set of data from the single non-volatile memory; storing the first set of data in the memory of the first one of the plurality of ICs (see Yamada FIG 6: S3 and COL 3 LINES 28-46);
- receiving, at the first one of the plurality of ICs, a second set of data from the single non-volatile memory; transmitting the second set of data from the first one of the plurality of ICs to the second one of the plurality of ICs; and storing the second set of data in the memory of the second one of the plurality of ICs; wherein the first and second sets of data comprise program code (see Yamada FIG 6: S5 and COL 3 LINES 28-46).

However, Yamada does not expressly disclose the plurality of ICs disposed on a printed circuit board.

In the same field of endeavor Stancil discloses it is well known to place many components on a motherboard (substrate) (see Stancil COL 5 LINES 5-10).

It would have been obvious to modify Yamada to integrate the components on a motherboard.

The suggestion/motivation for doing so would have been of higher performance system s (see Stancil COL 2 LINES 24-28).

Therefore it would have been obvious to modify Yamada to integrate the components on a motherboard for the benefit higher performance to arrive at the invention as specified in the claims.

However, Yamada and Stancil does not expressly disclose

- test circuitry for providing debugging functionality
- transmitting, using the debugging circuitry, the second set of data from the first one of the plurality of ICs to the second one of the plurality of ICs; and

In the same filed of endeavor Sun Microelectronics discloses

- test circuitry for providing debugging functionality (see Sun Microelectronics PAGE 2 FIG 1: Input Boundary Cell, Output Boundary Cell and PAGE 6 FIG 3),
- transmitting, using the debugging circuitry, the second set of data from the first one of the plurality of ICs to the second one of the plurality of ICs; and (see Sun Microelectronics PAGE 2 FIG 1: Input Boundary Cell, Output Boundary Cell and PAGE 6 FIG 3).

  [Placing the boundary scan cells at the input and output would necessarily entail the data be sent via the boundary scan cells.]

It would have been obvious to modify Yamada in view of Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by Sun Microelectronics.

The suggestion/motivation for doing so would have been for the benefit of a test interface and the use of an industry standard protocol (see Sun Microelectronics PAGE 1 Paragraph 1: "This capability enables in-circuit testing without the need bed-of-nails in-circuit testing equipment.").

Therefore it would have been obvious to modify Yamada and Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by Sun Microelectronics for the benefit of a test interface to arrive at the invention as specified in the claims.

As per claim 11, Yamada in view of Stancil and Sun Microelectronics discloses the method of Claim 10,

- further comprising: executing, in the first IC, at least a portion of the code in the program first set of data (see FIG 6: S6);
- receiving, at the first one of the plurality of ICs, a third set of data from the single non-volatile memory; transmitting the third set of data from the first one of the plurality of ICs to a third one of

the plurality of ICs; and storing the third set of data in the memory of the third one of the plurality of ICs (see Stancil FIG 2: 114, 116, 118);

As per claim 12. Yamada in view of Stancil and Sun Microelectronics disclose the method of Claim 10,

- wherein transmitting the second set of data from the first one of the plurality of ICs to the second one of the plurality of ICs comprises serially shifting data out of the first one of the plurality of ICs via an output terminal; wherein the output terminal is coupled to an input terminal of the second one of the plurality of ICs, the input terminal coupled to circuitry within the second one of the plurality of ICs that is adapted to receive serial data (see Yamada FIG 6: S5 SERIALLY).

As per claim 13, Yamada in view of Stancil and Sun Microelectronics disclose the method of Claim 12,

- further comprising placing the test circuitry in a test mode (see Sun Microelectronics PAGE 3 Paragraph 2) and
- providing transmitting control information from the first one of the plurality of ICs to the second one of the plurality of ICs prior to transmitting the second set of data (see Yamada FIG 6: S4).

As per claim 14, Yamada in view of Stancil and May disclose the method of claim 13.

- wherein the control information is transmitted in accordance with a JTAG standard of communication (see Sun Microelectronics Page 3: "JTAG Basics").

5. **CLAIMS 15-18** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Pat No. 5757639) in view of Stancil (US Pat No. 6272584) and Sun Microelectronics (NPL Introduction to JTAG Boundary Scan).

As per claim 15, Yamada discloses an electronic product, comprising: a first integrated circuit having a first processor (see Yamada FIG 1: 1), a first internal memory (see Yamada FIG 1: 3), a first serial communication interface (see Yamada FIG 1: "SERIAL COMMUNICATION"), and an external memory interface (see Yamada FIG 1: 4); an external memory coupled to the external memory interface (see FIG 1: 5 MEMORY CARD); a second integrated circuit having second processor (see FIG 1: 6), a second internal memory (see FIG 1: 8), and a second serial communication interface, the second serial communication interface being coupled to the first serial communication interface (see FIG 1: "SERIAL COMMUNICATION");

- wherein the first test circuit and the second test circuit are configured communicate code images in another mode (see Yamada FIG 6: S5 and COL 3 LINES 32-46).

However, Yamada does not expressly disclose wherein the first integrated circuit, the external memory, and the second integrated circuit are disposed on a substrate.

In the same field of endeavor Stancil discloses it is well known to place many components on a motherboard (substrate) (see Stancil COL 5 LINES 5-10).

It would have been obvious to modify Yamada to integrate the components on a motherboard.

The suggestion/motivation for doing so would have been of higher performance system s (see Stancil COL 2 LINES 24-28).

Therefore it would have been obvious to modify Yamada to integrate the components on a motherboard for the benefit higher performance to arrive at the invention as specified in the claims.

However, Yamda and Stancil does not expressly disclose

- a first test circuit
- a second test circuit

- wherein the first test circuit and the second test circuit are configured and arranged to communicate debugging information in a test mode.

In the same field of endeavor Sun Microelectronics discloses

However, Yamda and Stancil does not expressly disclose

- a first test circuit (see Sun Microelectronics PAGE 3 FIG 1 Input Boundary Cell and PAGE 6 FIG 3)
- a second test circuit (see Sun Microelectronics PAGE 3 FIG 1 Input Boundary Cell and PAGE 6 FIG 3)
- wherein the first test circuit and the second test circuit are configured and arranged to communicate debugging information in a test mode (see Sun Microelectronics PAGE 3 2nd Paragraph).

It would have been obvious to modify Yamada in view of Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by Sun Microelectronics.

The suggestion/motivation for doing so would have been for the benefit of a test interface and the use of an industry standard protocol (see Sun Microelectronics PAGE 1 Paragraph 1: "This capability enables in-circuit testing without the need bed-of-nails in-circuit testing equipment.").

Therefore it would have been obvious to modify Yamada and Stancil to communicatively couple the first and second integrated circuit through test circuitry as taught by Sun Microelectronics for the benefit of a test interface to arrive at the invention as specified in the claims.

As per claim 16, Yamada in view of Stancil and Sun Microelectronics disclose the electronic product of claim 15,

- wherein the first processor is coupled to the first internal memory, the first internal memory is adapted to receive a first code image (see Yamada FIG 6: S3), the second processor is coupled to the second internal memory, the second internal memory is adapted to receive a second code image (see Yamada FIG 6: S5), and the external memory is a non-volatile memory encoded with the first and second code images (see Yamada COL 2 LINES 50-57).

As per claim 17, Yamada in view of Stancil and Sun Microelectronics disclose the electronic product of claim 16,

- wherein the first integrated circuit includes a first hardware facility for performing at least a first function, and the second integrated circuit includes a second hardware facility for performing at least a second function, and the first and second functions are different (see Yamada COL 3 LINES 24-45).

As per claim 18, Yamada in view of Stancil and Sun Microelectronics disclose the electronic product of Claim 17, further comprising

- a third integrated circuit, having a third processor, a third internal memory, and a third serial communication interface, the third serial communication interface being coupled to the second serial communication interface, the third processor coupled to the third internal memory, the third internal memory is adapted to receive a third code image, and the external memory further encoded with the third code image (see Stancil FIG 2: 114, 116, 118).

  [Stancil discloses configuring plural processing devices using a single EEPROM.]

6. **CLAIMS 15-18** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Pat No. 5757639) in view of Stancil (US Pat No. 6272584) and Chang (US Pat No. 6484273).

As per claim 15, Yamada discloses an electronic product, comprising: a first integrated circuit having a first processor (see Yamada FIG 1: 1), a first internal memory (see Yamada FIG 1: 3), a first serial communication interface (see Yamada FIG 1: "SERIAL COMMUNICATION"), and an external memory interface (see Yamada FIG 1: 4); an external memory coupled to the external memory interface (see FIG 1: 5 MEMORY CARD); a second integrated circuit having second processor (see FIG 1: 6), a second internal memory (see FIG 1: 8), and a second serial communication interface, the second serial communication interface being coupled to the first serial communication interface (see FIG 1: "SERIAL COMMUNICATION");

- wherein the first test circuit and the second test circuit are configured communicate code images in another mode (see Yamada FIG 6: S5 and COL 3 LINES 32-46).

However, Yamada does not expressly disclose wherein the first integrated circuit, the external memory, and the second integrated circuit are disposed on a substrate.

In the same field of endeavor Stancil discloses it is well known to place many components on a motherboard (substrate) (see Stancil COL 5 LINES 5-10).

It would have been obvious to modify Yamada to integrate the components on a motherboard.

The suggestion/motivation for doing so would have been of higher performance system s (see Stancil COL 2 LINES 24-28).

Therefore it would have been obvious to modify Yamada to integrate the components on a motherboard for the benefit higher performance to arrive at the invention as specified in the claims.

However, Yamda and Stancil does not expressly disclose

- a first test circuit
- a second test circuit

- wherein the first test circuit and the second test circuit are configured and arranged to communicate debugging information in a test mode.

In the same field of endeavor Chang discloses an integrated circuit (see Chang FIG 1) including a test circuit (see Chang FIG 2: 54), wherein the test circuit is configured and arranged to communicate debugging information in a test mode (see COL 2 LINES 58-65) and to communicate code images in another mode (see Chang COL 2 LINES 1-10).

It would have been obvious to modify each of the first and second integrated circuits as taught by Yamda and Stancil to include a test circuit as taught by Chang.

The suggestion/motivation for doing so would have been for the benefit of a non-intrusive development and debug technology (see Chang COL 1 LINES 35-45).

Therefore it would have been obvious to modify Yamada and Stancil to implement a test circuit as taught by Chang for the benefit of debugging technology to arrive at the invention as specified in the claims.

As per claim 16, Yamada in view of Stancil and Chang disclose the electronic product of claim 15,

- wherein the first processor is coupled to the first internal memory, the first internal memory is adapted to receive a first code image (see Yamada FIG 6: S3), the second processor is coupled to the second internal memory, the second internal memory is adapted to receive a second code image (see FIG 6: S5), and the external memory is a non-volatile memory encoded with the first and second code images (see COL 2 LINES 50-57).

As per claim 17, Yamada in view of Stancil and Chang disclose the electronic product of claim 16,

- wherein the first integrated circuit includes a first hardware facility for performing at least a first function, and the second integrated circuit includes a second hardware facility for performing at least a second function, and the first and second functions are different (see COL 3 LINES 24-45).

As per claim 18, Yamada in view of Stancil and Chang disclose the electronic product of Claim 17, further comprising

- a third integrated circuit, having a third processor, a third internal memory, and a third serial communication interface, the third serial communication interface being coupled to the second serial communication interface, the third processor coupled to the third internal memory, the third internal memory is adapted to receive a third code image, and the external memory further encoded with the third code image (see Stancil FIG 2: 114, 116, 118).

[Stancil discloses configuring plural processing devices using a single EEPROM.]

IV. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Applicants' arguments filed 17 September 2009 have been fully considered.

RESPONSE TO AMENDMENTS/ARGUMENTS

1st ARGUMENT:

Having one port listed as a test intertace, one reasonable interpretation is that PLD controller 240 includes some test circuitry for the testing of the PLD controller 240. However, this reasoning does not extend to the erroneous conclusion that all paths through the PLD controller pass through test circuitry. If such were the case, any circuit having an externally accessible JTAG port would constitute testing circuitry regardless of actual function. Without further description, one skilled in the art could also reasonably conclude that the described port of PLD controller 240 is connected to an external "PLD test Interface," and the PLD controller includes no test circuitry. Applicant submits that the Office Action has not presented a convincing line of reasoning why a skilled artisan would understand that the '483 reference explicitly or implicitly suggests that first and second ICs of the '483 reference are coupled through test circuitry. See M.P.E.P §706.020). Because the Office Action has not particularly

Examiner respectfully disagrees.

As per MPEP 2125:

DRAWINGS CAN BE USED AS PRIOR ART

> Drawings and pictures can anticipate claims if they clearly show the structure which is claimed. In re Mraz, 455 F.2d 1069, 173 USPQ 25 (CCPA 1972). However, the picture must show all the claimed structural features and how they are put together. Jockmus v. Leviton, 28 F.2d 812 (2d Cir. 1928). The origin of the drawing is immaterial. For instance, drawings in a design patent can anticipate or make obvious the claimed invention as can drawings in utility patents. When the reference is a utility patent, it does not matter that the feature shown is unintended or unexplained in the specification. The drawings must be evaluated for what they reasonably disclose and suggest to one of ordinary skill in the art. In re Aslanian, 590 F.2d 911, 200 USPQ 500 (CCPA 1979). See MPEP § 2121.04 for more information on prior art drawings as "enabled disclosures."

As Applicants' have stated in the argument "Having one port listed as a test interface, one reasonable interpretation is that PLD controller 240 includes some test circuitry for the testing of the PLD controller 240." The claim broadly recites test circuitry and does not further specify any additional structure or function. Test circuitry is construed as circuitry pertaining to testing. The PLD controller contains test inputs and is therefore construed to meet the claimed test circuitry.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., 'all paths pass through the test circutry') are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

2nd ARGUMENT:

> Applicant respectfully traverses the § 103(a) rejections of claims 10-14 for similar reasons as that of claims 1-9. For example, none of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including, e.g., aspects of the claimed invention directed to transmitting using debugging circuitry. As stated above, the Office Action has not particularly shown support or provided reasoning for the conclusion that the portion of the cited PLD controller 240 of Figure 2 of the '483 reference used for communication between first and second ICs constitutes debugging circuitry. Therefore, a primafacie case of obviousness has not been made and the rejections cannot stand.

Examiner notes Sun Microelectronics is relied upon for the claimed feature.

3rd ARGUMENT:

> Applicant further traverses the 103 rejection of claim 4 because the cited combination of references lacks correspondence. For example, none of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including, e.g., aspects of the claimed invention directed to executing at least a portion of the first set of programming instructions prior to transmitting the second set of programming instructions to the second IC. Applicant submits that Figure 6 of the '639 reference cited in the Office Action does not disclose the execution of the first set of programming instructions prior to transmission of the second set of instructions to the second IC. In contrast, Figure 6 clearly shows that

the first set of instructions stored in the first IC (element $3 of Figure 6) is executed (element $6 of Figure 6) after transmitting the second set of instructions to the second IC (element $5 of Figure 6). See also Col. 2:50 through Col. 3:3 of the '639 reference. Because the asserted '639 reference does not disclose the aspects of the present invention as asserted in the Office Action, no reasonable interpretation of the asserted prior art, taken alone or in combination, provides correspondence. As such, a proper § 103 rejection has not been presented and Applicant requests that the rejection be withdrawn.

Examiner notes May is now relied upon to teach the claimed feature.

4th ARGUMENT:

Regarding claim 6, it is unclear how the cited Figure 2 of the '483 reference is interpreted as disclosing test circuitry of each of the ICs having a test input for a test mode signal. The Office Action has not particularly pointed out respective inputs for a test mode signal corresponding to the first and second ICs. Rather, the Office Action cites to only one input (PLD test interface of Figure 2). Further, the cited Figure 2 does not illustrate a data flow in which a test input received at the asserted input port would be forwarded to each of the first and second circuits. Nor has the Office Action asserted and provided reasoning that this functionality is either implicit or inherent. Regarding claims 10-14, for similar reasoning to that stated above, it is unclear how the cited Figure 2 of the '483 reference is interpreted as disclosing first and second ICs each having test circuitry for providing debugging functionality. Because the references fail to disclose these operable aspects, no reasonable combination of the references would provide correspondence for claims 6 or 10-14. As such, the § 103 rejections fail and Applicant requests that they be withdrawn.

Examiner notes Sun Microelectronics is relied upon for the claimed feature.

5th ARGUMENT:

Applicant further traverses the § 103 (a) rejection of claims 15-18 because the ' 639 reference either alone or in combination with the '273 and '584 references lacks correspondence. None of the asserted references alone or in combination appears to relate to the claimed invention when viewed "as a whole" (§ 103(a)) including aspects regarding first and second test circuits, each test circuit configured and arranged to communicate debugging information in a test mode and communicate code images in another mode. The '273 reference does not appear to disclose a test circuit that communicates debugging information in a test mode and communicates code images in another mode as asserted in the Office Action. In contrast the portions of the '273 reference cited in support of the rejection only disclose JTAG circuitry configured to communicate test data. Similar to the rejections of claims 1-9, the rejections of claims 15-18 appear to rely on the erroneous conclusion that the entire circuit shown in the cited Figure 2 of the '273 reference constitutes test circuitry merely because a JTAG module is provided in one portion of the circuit. Applicant submits that such an interpretation is contrary to the plain meaning of the claimed aspects of the invention.

Examiner respectfully disagrees. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Chang discloses 'a specialized debugging mode (see COL 2 LINES 58-67).' Yamada discloses during operation the first and second circuits communicate code images (see Yamada FIG 6: S5 and COL 3 LINES 32-46).

6th ARGUMENT:

> Further, the Office Action has not provided any motivation to arrange test circuits in each IC to communicate code images while in a non-testing mode. Applicant submits that the Examiner has simply identified JTAG circuitry as common circuit elements (which can be found in any number of references) and then arranged these elements, using the claimed invention as a template, to provide testing circuitry arranged to communicate code images while in a non-testing mode. This is the hallmark of improper hindsight reconstruction with the proposed combination being derived, not "on the basis of the facts gleaned from the prior art," but solely from Applicant's disclosure. See, e.g., M.P.E.P. § 2142. As explained in M.P.E.P. § 2143, "(t)he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." As JTAG circuitry is not taught to be used in the manner claimed nor is there any suggestion toward this end in the references, the rejection cannot stand and there is not aprimafacie case of obviousness.

Examiner respectfully disagrees. As stated above the suggestion/motivation for doing so would have been for the benefit of a non-intrusive development and debug technology (see Chang COL 1 LINES 35-45).

Applicants are arguing patentability on the grounds that, unlike Yamada, the claimed invention provides a testing interface for each circuit. Providing a testing interface for each circuit, as Applicants' have claimed, is well known and the motivation for doing so is self-evident (i.e., provide debug capabilities). Merely providing testing interface for each circuit is not deemed non-obvious.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and

does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper.

See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

7th ARGUMENT:

> In response to the objection to the drawings, Applicant submits that the objection is improper and not required under 37 C.F.R. 1.83(a). In support of Applicant's position reference is made to 35 USC §113 and M.P.E.P. § 601.01(f), which indicate that "applicant shall furnish a drawing where necessary for the understanding of the subject matter sought to be patented." The Office Action has not indicated why one skilled in the art would not be able to understand the claimed invention. In addition, M.P.E.P. § 601.01(f) indicates that it has been PTO practice to treat an application that contains at least one process or method claim as an application for which a drawing is not necessary for an understanding of the invention under 35 USC §113. Since most of the claims in the current application are method claims, Applicant has complied with M.P.E.P. § 601.01(0.

Examiner initially notes the objection was made under 37 C.F.R. 1.83 (a). Arguing the drawings are compliant with 35 USC 113 does not address the deficiency under 37 C.F.R. 1.83 (a).

37 C.F.R. 1.83 (a) states in part:

> The drawing in a nonprovisional application must show every feature of the invention specified in the claims. However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box). In addition, tables and sequence listings that are included in the specification are, except for applications filed under 35 U.S.C. 371, not permitted to be included in the drawings.

The drawings do not show every feature of the invention specified in the claims. As per 37 C.F.R. 1.83 (a) conventional features must be illustrated in the drawings. The drawing objection may be overcome by illustrating the integrated circuits having test circuitry, and further illustrating the transmission path goes through the test circuitry as recited in the claims but not illustrated in the drawings.

V. CLOSING COMMENTS

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

Va. CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-18 have received a third action on the merits and are subject of a final office action.

For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

VI. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kalpit Parikh whose telephone number is (571) 270-1173. The examiner can normally be reached on MON THROUGH FRI 7:30 TO 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christian Chace can be reached on (571) 272-4190. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BRP/kp /KP/
4 February 2010

/Brian R. Peugh/
Primary Examiner, Art Unit 2187
February 5, 2010